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09/746,068	12/26/2000	Hisashige Ando	1614.1107	1994

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/746,068	ANDO, HISASHIGE
	Examiner	Art Unit
	Shane F Gerstl	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-11 and 13-16* is/are rejected.

7)☒ Claim(s) *3,4 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Received

2. Receipt is acknowledged of extension of time and amendment papers submitted, where the papers have been placed of record in the file.

3. The amendment filed 11 March 2004 has successfully overcome the objections to the title, drawings, and claims as well as the 35 USC 112 rejections whereby the objections and rejections have been withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Helenius (4,395,758).

6. In regard to claim 1, Helenius discloses an information-processing device (figure 2) that executes a specific process more frequently than other processes among a variety of processes said information-processing device comprising:

a. a first processor configured to execute an entire instruction set corresponding to the variety of processes; Column 2, lines 30-45 show a central

processor or first processor for processing a number of instructions (an entire instruction set).

b. a second processor configured to execute a portion or entirety of the same instruction set that the first processor executes, said second processor being capable of executing a part of said instruction set corresponding to the specific process more efficiently than said first processor; This section also shows that a special processor processes certain of those instructions (a portion of the same instruction set). This processor is the floating point accelerator mentioned in column 12, lines 19-23 and column 13, lines 17-19 that processes these special instructions (floating point instructions) more efficiently, especially when extensive floating point instructions are used (the more frequently executed specific process as opposed to the other instructions).

c. wherein said second processor executes the specific process whereas said first processor executes the other processes, as shown above.

7. In regard to claim 2, Helenius discloses the information-processing device as claimed in claim 1, as shown above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor by interrupting said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed. Column 2, lines 37-43 show that all operands (and thus the processes) are allocated to the special processor. If the special processor determines that the

instructions are special instructions (floating point) that it should execute, it inhibits or interrupts the first processor from processing the operation.

8. In regard to claim 6, Helenius discloses the information-processing device as claimed in claim 1, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. The abstract shows that the central processor has general purpose registers and is thus a general purpose processor. Figure 9 shows that the special processor (100) performs transactions with the central processor and thus is a transaction processor.

9. In regard to claim 7, Helenius discloses the information-processing device as claimed in claim 1, as described above, wherein said first processor and said second processor share a memory space. As shown in the section cited above, the processor and special processor receive instruction information of the same instruction at the same time and thus are accessing the same memory.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5, 8-11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Helenius in view of Hennessy.

12. In regard to claim 5,

a. Helenius discloses the information-processing device as claimed in claim 1, as described above, wherein said second processor is capable of executing the part of said instruction set corresponding to the specific process more efficiently than said first processor (as described above)

b. Helenius does not disclose that the second processor executes the specific process more efficiently by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the second processor a multiprocessor as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

13. In regard to claim 8,

a. Helenius discloses the information-processing device as claimed in claim 1, as described above,

b. Helenius does not disclose wherein said information-processing device includes a plurality of first processors and second processors.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

14. In regard to claim 9,

a. Helenius discloses an information-processing device (figure 2) that executes a specific process more frequently than other processes among a variety of processes said information-processing device comprising:

i. a first processor configured to execute an entire instruction set corresponding to the variety of processes; Column 2, lines 30-45 show a

central processor or first processor for processing a number of instructions (an entire instruction set).

ii. a second processor configured to execute a portion or entirety of the same instruction set that the first processor executes, said second processor being capable of executing a part of said instruction set corresponding to the specific process more efficiently than said first processor; This section also shows that a special processor processes certain of those instructions (a portion of the same instruction set). This processor is the floating point accelerator mentioned in column 12, lines 19-23 and column 13, lines 17-19 that processes these special instructions (floating point instructions) more efficiently, especially when extensive floating point instructions are used (the more frequently executed specific process as opposed to the other instructions).

iii. wherein said second processor executes the specific process whereas said first processor executes the other processes as shown above.

b. Helenius does not disclose that the second processor is capable of executing multiples of a specific process concurrently.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel. This means that if applied to the

system of Helenius, the process that the second processor executes would be run on multiple processors, or multiples of the process would be executed.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

15. In regard to claim 10, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as shown above, wherein all the processes are allocated to said second processor initially, wherein said second processor passes a given process to said first processor in a case in which an instruction other than the part of the instruction set corresponding to the specific process must be executed. Column 2, lines 37-43 show that all operands (and thus the processes) are allocated to the special processor. If the special processor determines that the instructions are special instructions (floating point) that it should execute, it inhibits or interrupts the first processor from processing the operation.

16. In regard to claim 11, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein all the processes

are allocated to said second processor initially, wherein said second processor passes a given process to said first processor when an instruction that cannot be executed appears or the execution of the process is judged not efficient by said second processor in said given process. Since the second processor would have decided to execute the instruction and inhibit the first processor and because the architecture of the patent is designed for the second processor to more efficiently process the special instructions than the first processor, when the second processor does not inhibit the first processor and sends the operands to the first processor, the second processor inherently judges the process not efficient.

17. In regard to claim 13,

a. Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said second processor is capable of executing all or part of said instruction set corresponding to the specific process more efficiently than said first processor (as described above)

b. Helenius in view of Hennessy does not disclose that the second processor executes the specific process more efficiently by executing said specific process in parallel by use of at least one of a multi-threading method and a multi-processing method.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing. It is defined page 712, last paragraph that a parallel processing program is a program that runs on multiple processors, thus the processors run in parallel.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius in view of Hennessy to make the second processor a multiprocessor as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius in view of Hennessy to make the second processor execute in parallel by making it a multiprocessor as taught by Hennessy so that execution is faster and more efficient.

18. In regard to claim 14, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor is a general-purpose processor, wherein said second processor is a transaction processor designed to efficiently execute a transaction process as the specific process. The abstract shows that the central processor has general purpose registers and is thus a general purpose processor. Figure 9 shows that the special processor (100) performs transactions with the central processor and thus is a transaction processor.

19. In regard to claim 15, Helenius in view of Hennessy discloses the information-processing device as claimed in claim 9, as described above, wherein said first processor and said second processor share common memory address space. As shown in the section cited above, the processor and special processor receive

instruction information of the same instruction at the same time and thus are accessing the same memory.

20. In regard to claim 16,

a. Helenius discloses the information-processing device as claimed in claim 9, as described above,

b. Helenius does not disclose wherein said information-processing device includes a plurality of first processors and second processors.

c. Hennessy has disclosed on page 718 in figure 9.2 a multiprocessor for increasing efficiency by parallel processing.

d. Hennessy has taught on page 712 that computers are made more powerful by connecting many small ones or by multiprocessing. It also says that multiprocessors may be faster than the fastest uniprocessor. This notable processing speed increase would have motivated one of ordinary skill in the art to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Helenius to make the first and second processors multiprocessors as taught by Hennessy so that execution is faster and more powerful.

Response to Arguments

21. Applicant's arguments, see pages 8-10, filed 11 March 2004, with respect to the rejection(s)of claim(s) 1 and 9 under 35 USC 102(e) and 35 USC 103(a) respectively have been fully considered and are persuasive. Therefore, the rejection has been

withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Helenius.

22. In response to applicant's argument on pages 9-10 that there is no suggestion to combine the references Evoy and Hennessy (similar to the now Helenius in view of Hennessy), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Hennessy provides the motivation on page 712, as stated in the previous Action and as admitted by Applicant on page 9, that connecting multiple computers increases processing power. Since in the art increasing processing power or speed is a common goal, there is adequate motivation to make the slave processor of Evoy or Helenius a multiprocessor.

Allowable Subject Matter

23. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach the second processor interrupting the first processor to execute a process when the second processor cannot execute or efficiently execute the process. Instead, the first processor is simply not inhibited in doing so. In addition, no prior art of record suggests that it

would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record so the second processor interrupts the first processor to execute a process when the second processor cannot execute or efficiently execute the process.

24. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach that the process the second instruction cannot execute efficiently is a floating point process. Instead, the second processor does efficiently execute these processes. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record so the process the second instruction cannot execute efficiently is a floating point process.

25. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not specifically teach that the process the second instruction cannot execute efficiently is a floating point process. Instead, the second processor does efficiently execute these processes. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the art at the time of invention to modify the prior art of record so the process the second instruction cannot execute efficiently is a floating point process.

Conclusion

26. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited in the previous Office Action remain relevant and thus are cited herein as well.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

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May 17, 2004

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